Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUCTIONS:**

1. **OUTPUT A**
2. **INPUT A-**
3. **INPUT A+**
4. **GND**
5. **INPUT B+**
6. **INPUT B-**
7. **OUTPUT B**
8. **V+**

**.033”**

**.034”**

**7 8 1**

**5**

**6**

**3**

**2**

**4**

**1**

**9**

**3**

**C**

**DIE ID**

**MASK REF**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential: FLOATING**

**Mask Ref: 193 C**

**APPROVED BY: DK DIE SIZE .033” X .034” DATE: 9/22/21**

**MFG: NATIONAL THICKNESS .015” P/N: LM193**

**DG 10.1.2**

#### Rev B, 7/1